PROCESS FOR REDUCING THE ELECTRICAL CONSUMPTION OF A TRANSMITTER/RECEIVER OF DIGITAL INFORMATION, IN PARTICULAR A CELLULAR MOBILE TELEPHONE, AND CORRESPONDING TRANSMITTER/RECEIVER

Field of the Invention

The present invention relates to a wireless transmission of digital information, especially for a cellular mobile telephone, and in particular, a

5   cellular mobile telephone operating according to the Universal Mobile Terrestrial Standard (UMTS) standard.

Background of the Invention

A cellular mobile telephone has two modes of operation, an active mode and an idle mode. In the

10   active mode, which corresponds to an exchange of dialog during the course of a communication established between the base station and the cellular telephone, the transmission and reception pathways of the telephone are both used to transfer voice or digital

15   data between a base station and the telephone.

Outside of a telephone communication, the cellular telephone stands by in the idle mode. In the idle mode, the transmission and/or reception pathways are activated and deactivated at regular intervals to

20   maintain a regular connection with the base station.

From a structural point of view, apart from the transmission/reception stage, which comprises the transmission pathway and the reception pathway, the cellular telephone comprises a processing stage

5   connected to the transmission/reception stage and comprises means for digital modulation/demodulation. The means for digital modulation/demodulation may be partly provided using hard-wired logic and partly provided using software within a signal processor. This

10   processor thus performs, in particular, the demodulation of the signal received and the modulation of the signal to be transmitted.

Moreover, various reference signals having chosen frequencies and clock signals must be generated

15   and delivered respectively to the transmission pathway, to the reception pathway and to the modulation/ demodulation processor. The frequencies of the reference signals fix or set the transmission and reception frequencies.

20   The various reference signals and clock signals are delivered by a frequency synthesizer stage controlled by automatic frequency control means. The accuracy required with respect of the transmission frequency is typically ± 0.1 ppm for a nominal

25   frequency in the 2 GHz range.

Currently, the internal architecture of the frequency synthesizer stage of a cellular mobile telephone is composed of conventional phase-locked loops which generate at the output of the oscillators

30   the reference signals intended for the transmission/reception stage as well as the clock signal intended for the modulation/demodulation means.

The base signal intended for these phase-locked loops, which forms a frequency reference, is generated a controlled oscillator, such as a temperature-stable voltage-controlled oscillator (VTCXO oscillator), for example, having the required accuracy of about ± 0.1 ppm. This oscillator conditions the accuracy demanded, and in particular, with respect to the transmission frequency.

On the basis of this architecture, the controlled oscillator is always operating, as is the phase-locked loop generating the clock signal for the modulation/demodulation means and the loop generating the reference signal for the transmission pathway. However, such a structure exhibits drawbacks. Specifically, not only is a controlled oscillator of this kind expensive, but its electrical consumption impairs the autonomy of the telephone.

Summary of the Invention

An objective of the present invention is to optimize the electrical consumption of the transmitter/receiver (telephone) by optimizing the frequency synthesizer stage as a function of the operating mode of the cellular telephone.

A particular objective of the present invention is the generation of the various clock and synchronization signals in the various operating modes of the transmitter/receiver for reducing electrical consumption.

The invention therefore provides a process for reducing the electrical consumption of a transmitter/receiver of digital information, in particular, a cellular mobile telephone. The

transmitter/receiver comprises a frequency synthesizer
stage controlled by an automatic frequency control
algorithm. This frequency synthesizer stage is able to
deliver at least one reference signal of a chosen

5 frequency to the transmission/reception stage of the
transmitter/receiver, and a master-clock signal of a
chosen frequency to the modulation/demodulation means
of the transmitter/receiver.

According to a general characteristic of the

10 invention, the reference signal or signals are
generated with a predetermined accuracy (termed the
transmission accuracy), typically ± 0.1 ppm, on the
basis of at least a first fractional-division phase-
locked loop controlled by the automatic frequency

15 control algorithm. This loop receives from a quartz
oscillator, for example, a base signal having a
predetermined base frequency and a base accuracy lower
than the transmission accuracy. The base accuracy is
typically on the order of ± 10 ppm.

20 A clock signal is generated with a
predetermined accuracy (generally also the transmission
accuracy), on the basis of a second fractional-division
phase-locked loop controlled by the automatic frequency
control algorithm, which also receives the base signal.

25 When the transmission/reception stage is
inactive (for example, in idle mode), the second
fractional-division phase-locked loop is rendered
inactive, with the base signal then being the master-
clock signal. When the transmission/reception stage is

30 active, the second loop is activated with the clock
signal generated by this second loop then being the
master-clock signal.

Stated otherwise, the power consumption of the telephone is reduced by using fractional-division phase-locked loops receiving a frequency reference from a fairly inaccurate quartz oscillator, and by switching

5 the output of the oscillator onto the input of the processing stage when the transmission/reception stage is inactive. The loops may then be deactivated.

More precisely, when the transmission/ reception stage, for example the transmission pathway,

10 has to be activated in an active mode during a telephone communication or else in an idle mode at regular intervals, the modulation/demodulation means of the telephone control the second phase-locked loop (and of course the first loop or loops) by way of the

15 automatic frequency control algorithm by demodulating a pilot signal transmitted by the base station. This is for allowing generation of a very accurate transmission reference frequency, typically ± 0.1 ppm. The transmission reference frequency is intended for the

20 transmission pathway, and the generation of the master-clock signal of the signal processor.

Conversely, when the transmission/reception stage is inactive at regular intervals during the idle mode, it is unnecessary to generate a reference signal

25 for the transmission pathway. Only the signal processor needs to be activated. Also, in this case, it has been observed that it is unnecessary to activate the second phase-locked loop. Specifically, a master-clock signal of lower accuracy, for example ± 10 ppm,

30 proves to be quite sufficient to operate the processing stage. Also, this fairly inaccurate clock signal can then be delivered directly by a quartz reference oscillator, for example.

The invention results in particular from the observation that there exists, instants in the course of which it is unnecessary to formulate very accurate reference signals and clock signals since the

5   transmission/reception stage, and in particular the transmission pathway, is inactive. This is so since, in the course of these instants, a clock signal of lower accuracy is sufficient to operate the processing stage.

10   The invention also results from the observation that when the transmission/reception stage needs to be activated, the modulation/demodulation means and the automatic frequency control algorithm can commence operating with a fairly inaccurate clock

15 signal. This operation continues until the various fractional-division phase-locked loops are locked onto accurate frequencies with an accuracy on the order of $\pm$ 0.1 ppm, following synchronization to a pilot signal.

Finally, in combination with these

20 observations, the invention uses fractional-division phase-locked loops which exhibit the feature of being able to deliver signals at an output with very high accuracies, for example, on the order of a few hertz. This is on the basis of a base reference signal

25 delivered, for example, by a quartz oscillator of lower accuracy than that of a VTCXO oscillator, but conversely exhibiting lower electrical consumption than that of the VTCXO oscillator.

The invention also proposes a transmitter/

30 receiver, in particular, a cellular mobile telephone, comprising a transmission/reception stage, a processing stage connected to the transmission/reception stage and comprising modulation/demodulation means and automatic

frequency control means, and a frequency synthesizer
stage controlled by the automatic frequency control
means for delivering at least one reference signal of a
chosen frequency to the transmission/reception stage,

5   and a master-clock signal of chosen frequency to the
modulation/demodulation means.

According to a general characteristic of the
invention, the frequency synthesizer stage comprises at
least a first fractional-division phase-locked loop

10 whose output, linked to the transmission/reception
stage, is able to deliver with a predetermined
transmission accuracy the reference signal, and a
second fractional-division phase-locked loop whose
output is able to deliver with a predetermined accuracy

15 a clock signal.

Each loop is able to adopt on command an
active state and an inactive state, and has a control
input linked to the automatic frequency control means.
Each loop also has an input for receiving a base signal

20 emanating from an oscillator that has a predetermined
base frequency and a base accuracy lower than the
transmission accuracy.

The frequency synthesizer stage moreover
comprises controllable switching means possessing a

25 first state linking the output of the oscillator to the
modulation/demodulation means, and a second state
linking the output of the second loop to the
modulation/demodulation means.

Moreover, the transmitter/receiver

30 furthermore comprises control means for placing the
second loop in an inactive state and the switching
means in their first state, and to place the second

loop in an active state and the switching means in their second state.

According to one embodiment of the invention, each loop is a delta-sigma modulation fractional-division phase-locked loop. This allows for a decrease in the phase noise of electrical origin and a clock accuracy on the order of a few hertz.

Brief Description of the Drawings

Other advantages and characteristics of the invention will become apparent on examining the detailed description of modes of implementation and embodiments, which are in no way limiting, and of the appended drawings, in which:

Figure 1 is a block diagram illustrating the internal architecture of part of a cellular mobile telephone, and more particularly, the internal architecture of a frequency synthesizer stage according to the present invention;

Figure 2 is a block diagram of a fractional-division phase-locked loop according to the present invention;

Figure 3 illustrates an alternative embodiment using a delta-sigma modulation to control the divider of a fractional-division phase-locked loop according to the present invention; and

Figure 4 illustrates a mode of implementation of a process according to the present invention.

Detailed Description of the Preferred Embodiments

It is now assumed, while referring to Figure 1, that the invention applies in particular to the field of cellular mobile telephones, such as those

intended to operate according to the UMTS standard, for example.

A transmitting or base station, not represented in Figure 1 for the sake of simplification, 5 typically comprises a coding block receiving the useful data to be transmitted, for example speech, and performs in particular channel coding processing operations which are conventional and well known to the person skilled in the art. The output of this coding 10 block includes binary information blocks. The coding block is conventionally followed by a modulator performing, for example, a quadrature modulation of the QPSK type, according to terminology well known to the person skilled in the art, and transforms the binary 15 signal into an analog signal. This analog signal is then filtered in a transmission filter before being transmitted towards the telephones via an antenna, after having been transposed to a radiofrequency (RF).

The cellular mobile telephone TP comprises at 20 the front end an antenna ANT coupled to an analog transmission/reception stage which comprises a reception pathway RXC and a transmission pathway TXC. In the UMTS standard, the reception frequency can lie between 2110 and 2170 MHz, while the transmission 25 frequency, which is different from the reception frequency, can lie between 1920 and 1980 MHz.

Moreover, one of the requirements of the UMTS standard includes high accuracy of the transmission frequency. Specifically, by way of indication, this 30 transmission frequency must not vary by more than 0.1 ppm on either side of the nominal transmission frequency.

The transmission/reception stage is coupled
in a conventional manner, by way of an analog/digital
conversion stage CAN and a digital/analog CNA
conversion stage, to a digital processing stage. The
5   digital processing stage is formed partly by hard-wired
logic and partly by a signal processor DSP, for
example. The various functions of the DSP are then
carried out in software.

Operationally, the processing stage comprises
10   modulation/demodulation means MDM capable of performing
the demodulation of the signal received and the
modulation of the signal to be transmitted. This is
apart from the means for estimating the impulse
response of the transmission channel, means for
15   suppressing intersymbol interference (equalizer), and a
channel decoding block.

The portable telephone TP moreover comprises
at least one fractional-division phase-locked loop EPLL
intended to generate and deliver to the reception
20   pathway RXC and to the transmission pathway TXC
reference signals respectively having the nominal
reception and transmission frequencies. In the case
where the telephone comprises just a single loop EPLL
directly delivering the reference signal to one of the
25   transmission and reception pathways, there is then
provided a frequency shifting means for delivering the
reference signal to the other of the transmission and
reception pathways on the basis of the reference signal
delivered directly by the loop EPLL. Depending on the
30   architecture used for the telephone, it is possible to
provide two separate loops EPLL respectively delivering
two reference signals to the transmission pathway and

to the reception pathway, thus directly fixing or
setting the transmission and reception frequencies.

In the subsequent text, for the sake of
simplification, it will be assumed here that there is a
5 single loop EPLL. Everything described below is also
valid in the case where there are several loops EPLL.
The accuracy of the reference signal delivered by the
loop EPLL is controlled by a control signal SC1, which
is a digital word delivered by software from the
10 automatic frequency control AFC. More precisely, the
demodulation means MDM performs a demodulation of a
pilot signal transmitted by the base station on a pilot
channel having a predetermined frequency and containing
a predetermined code.

15   During demodulation of the pilot signal, the
demodulator uses a master clock signal generated, as
will be seen in greater detail below, by a phase-locked
loop MCPLL. The frequency of this master clock signal
must theoretically be a multiple of the data
20 transmission rate on the pilot channel (chip rate). If
this is not the case, during demodulation a rotation of
the modulation will be observed at a frequency
corresponding to the discrepancy between the
theoretical transmission rate (chip rate) and the
25 master clock signal. The automatic frequency control
algorithm will then adjust the value of the control
word to stop the rotation. In this case, all the
phase-locked loops of the telephone will then be
regarded as latched, and the various clocks will have
30 the required accuracy.

An automatic frequency control algorithm of
this kind is well known to the person skilled in the
art. The latter will in particular be able to refer to

the article by Aldo N. D'Andrea, entitled "Design of
Quadricorrelators for Automatic Frequency Control
Systems," IEEE Transactions on Communications, Vol. 41,
No. 6, June 1993. In addition, reference may be made

5   to the article by Wen-Yi Kuo, entitled "Frequency
Offset Compensation of Pilot Symbol Assisted Modulation
in Frequency Flat Fading," IEEE Transactions on
Communications, Vol. 45, No. 11, November 1997, or the
article by Bellini, entitled "Digital Frequency

10 Estimation in Burst Mode QPSK Transmission," IEEE
Transactions on Communications, Vol. 38, No. 7, July
1990.

Apart from the loop or loops EPLL, the
telephone also comprises another fractional-division

15 phase-locked loop MCPLL, whose output is linked to the
second input E2 of a switching means MCM with two
stages, for example, a multiplexer with two inputs and
one output. The output S of the switching means MCM is
linked to the modulation/demodulation means and

20 delivers a master-clock signal SHM to these means.

The means MCM moreover comprises a first
input E1 linked to the output of a quartz oscillator QT
having a predetermined base frequency, for example,
20 MHZ, and a much lower accuracy than the accuracy

25 required for the transmission frequency. In this
instance, the accuracy of the quartz oscillator is on
the order of ± 10 ppm.

The switching means MCM are controlled by a
control signal SCAI delivered by control means MCD.

30 The control means MCD are also software means. They
can also activate or disable the operation of the loops
EPLL and MCPLL with another control signal SCAC.

The signal SBA emanating from the oscillator also serves as reference signal for the phase-locked loops EPLL and MCPLL. The control signal SC2, which controls the accuracy of the clock signal SH delivered

5   by the loop MCPLL, is also delivered by the automatic frequency control means AFC and is also a digital word, which is linked in a fixed ratio to the control word SC1.

The structure of a fractional-division phase-

10   locked loop is fully known to the person skilled in the art, and the latter may in particular refer to the article entitled "Technique Enhances the Performance of PLL Synthetisers," Microwaves & RF, January 1993, pages 59-65. Figure 2 in this article recalls the essential

15   elements thereof.

More precisely, a fractional-division phase-locked loop PLLF comprises at the front end a phase and frequency detector PFD of conventional structure fully known to the person skilled in the art. The output of

20   this detector PFD drives a loop filter FT whose output is linked to the input of a voltage-controlled loop oscillator VCO. The frequency of the loop oscillator VCO is substantially the output frequency desired for the output signal delivered at the output SO of the

25   loop, which is the output of the oscillator VCO.

The output of the oscillator VCO is looped back to one of the inputs of the detector PFD by way of a fractional divider DV controlled by the control word SC emanating from the automatic frequency control means

30   AFC. The other input of the detector PFD receives the base signal SBA emanating from the oscillator QT.

The number N is the integer closest, but less than the ratio of the frequency of the signal SBA to

the frequency of the loop oscillator VCO. Moreover,
the ratio of the frequency of the signal SBA to the
accuracy required defines the number of bits of the
control word SC. Thus, by way of example, if the
5   output frequency of the loop needs to be equal to 2 GHz
with ± 0.1 ppm, this corresponds to an accuracy of
200 Hz, and if the frequency of the signal SBA is
20 MHz, the aforesaid ratio is equal to 20 MHz/200 Hz,
i.e. 100,000, this lying between 2^{16} and 2^{17}. The
10   control word SC will therefore be a 17-bit word which
will define the number of times that the divider DV
will perform a division by N and the number of times
that the divider DV will perform a division by N+1, to
attain the exact ratio between the signal SBA and the
15   output signal SO to within ± 0.1 ppm.

       A fractional-division phase-locked loop
therefore makes it possible to obtain very good
accuracy in the output frequency by using a base signal
emanating from an oscillator having a much lower
20   accuracy, and via the control of a divider with a
sufficiently long digital word.

       As a variation, as illustrated in Figure 3,
the control of the divider can result from a delta-
sigma modulation, also well known to the person skilled
25   in the art. By way of indication, the control word SC
arising from the means AFC drives an integrator. The
output of the integrator is then delivered via a filter
FT1 to the input of a quantization means QT. The
output of the quantization means QT is looped back to
30   the input of the integrator and controls the divider DV
of the phase-locked loop.

       Delta modulation is based on quantization of
the modification of the signal sample by sample, rather

than on quantization of the absolute value of the
signal at each sample. The name delta-sigma is given
to the modulator because of the presence of the sigma
integrator. A delta-sigma modulator is designed to
5 eliminate the quantization noise from the baseband.
Control of the divider by a delta-sigma modulation
allows a reduction in noise overall.

The person skilled in the art will be able to
refer for greater detail regarding an exemplary delta-
10 sigma modulation phase-locked loop to the article by
Perrott, entitled "A 27-mW CMOS Fractional-N
Synthesizer Using Digital Compensation for 2.5-Mb/s
GFSK Modulation," IEEE Journal of Solid-State Circuits,
Vol. 32, No. 12, December 1997, as well as to the above
15 referenced article entitled "Technique Enhances the
Performance of PLL Synthetisers."

The manner of operation of the frequency
synthesizer stage of the telephone according to the
invention will now be described in greater detail while
20 referring more particularly to Figure 4. In the active
mode, that is to say during a communication between the
base station BS and the telephone, the control means
MCD activates the phase-locked loops EPLL and MCPLL and
places the switching means MCM in their second state
25 linking the second output E2 to the output S.
Consequently, the master-clock signal SHM delivered to
the modulation/ demodulation means is the clock signal
SH delivered by the loop MCPLL. That is, a multiple of
the pilot signal transmission rate (chip rate), for
30 example 15.36 MHz for a transmission rate (chip rate)
equal to 3.84 Mcps as in the UMTS standard.

The accuracy of the signal SHM and of the
reference signals delivered to the transmission/

reception stage is then equal to ± 0.1 ppm. This accuracy is controlled by the control words SC1 and SC2 through the automatic frequency algorithm. In the idle mode, as illustrated in Figure 4, the base station BS

5   communicates at regular intervals with the portable telephone TP, with the pilot signal SP being transmitted at all times.

Outside of the periods of dialog between the base station BS and the telephone TP, the control means

10 MCD renders the loops EPLL and MCPLL inactive and places the switching means MCM in their first state linking the first input E1 with the output S. In this case, the master-clock signal SHM delivered to the processing stage is the base signal SBA delivered by

15 the oscillator QT. Consequently, the processing stage, and in particular the modulation/demodulation means, receives a clock signal whose accuracy is equal to that of the oscillator QT, namely in this instance ± 10 ppm. However, this accuracy is quite sufficient in the

20 course of these periods of non-dialog.

On the other hand, just before each period of dialog between the base station BS and the portable telephone, the control means MCD renders the loops EPLL and MCPLL active and places the switching means MCM in

25 their second state again. At the start of the activation of the loop MCPLL, the signal SHM (signal SH) is delivered with an accuracy of ± 10 ppm. However, this accuracy is sufficient to allow the automatic frequency control means AFC to perform the

30 frequency control and to deliver the control words SC1 and SC2. This is done to bring the accuracy to ± 0.1 ppm at the end of the duration DT. That is, when the dialog with the base station actually commences.

Typically DT may be on the order of a few microseconds depending on the architecture used. At the end of the dialog period, the control means deactivates the loops EPLL and MCPLL again and sets the switching means MCM

5   back into their second state.